A STABLE 2-26.5 GHz TWO-STAGE DUAL-GATE DISTRIBUTED MMIC AMPLIFIER

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Abstract

A 2 to 26.5 GHz monolithic distributed amplifier with 18.75 ± 1.25 dB of gain, better than 12 dB return losses at input and output, and greater than 40 dB of isolation has been realized on a single 3.02mm x 1.62mm chip.

Introduction

Distributed amplifiers in MMIC form have demonstrated very wide bandwidth performance [1,2,3,4]. In addition, distributed amplifiers are capable of very good input and output matches, excellent flatness, and, thus, cascadable. They are also less sensitive to process parameter variations than reactively matched amplifiers, which makes them especially suitable for monolithic intergration.

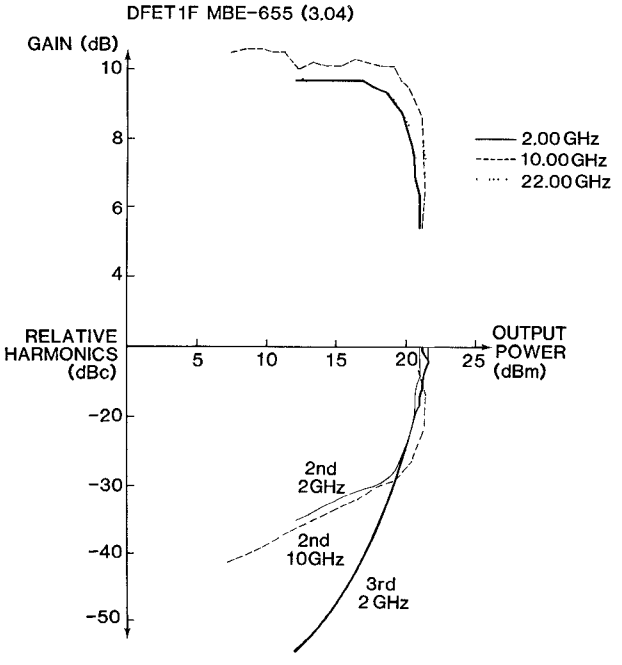

Fig. 1 Gain Compression and Relative Harmonics of a DFET1F.

Circuit Performance

The gain of a single stage dual-gate distributed amplifier (called DFET1F) was measured to be 9 ± .5 dB from 1.5 to 26.5 GHz with 19 dBm of output power with better than 25 dBc harmonics at the 1dB of gain compression point. The saturated output power was 21 dBm, as shown in Fig. 1. The noise figure of a DFET1F stage biased at 48% of I_{dss} was less than 9.3 dB, with an associated gain of 8 to 7 dB from 4 to 18 GHz, however the associated gain dropped to 6 dB at 26.5 GHz. The small signal gain and noise figure of the single stage DFET1F are shown in Fig. 2.

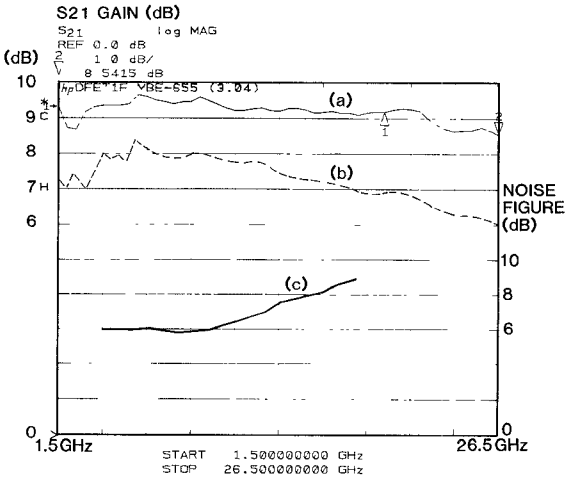

Fig. 2 Gain and Noise Figure of a single DFET1F.
(a) Gain at V_{DD} = 5.5 Volts, I_{DD} = 157 ma
(b) Gain at V_{DD} = 5.5 Volts, I_{DD} = 75 ma
(c) NF at V_{DD} = 5.5 Volts, I_{DD} = 75 ma

A dual-gate, two-stage distributed amplifier (called the DFET2F) has been fabricated in which a gain of 18.75 dB ± 1.25 dB has been achieved from 1.5 to 26.5 GHz, with input and output return losses better than 12 dB, and greater than 40 dB of isolation.

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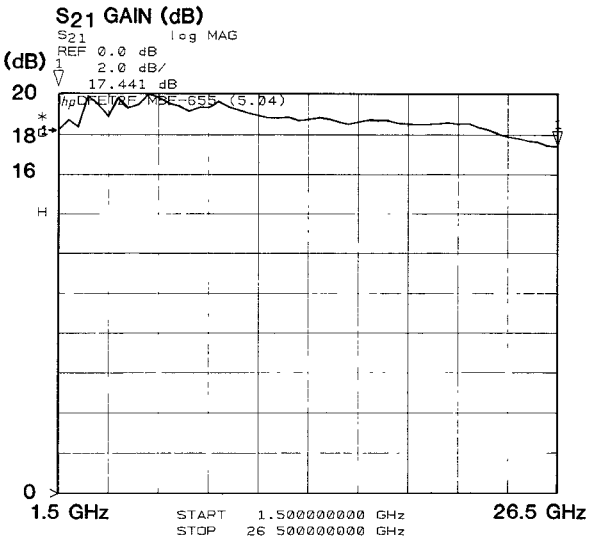
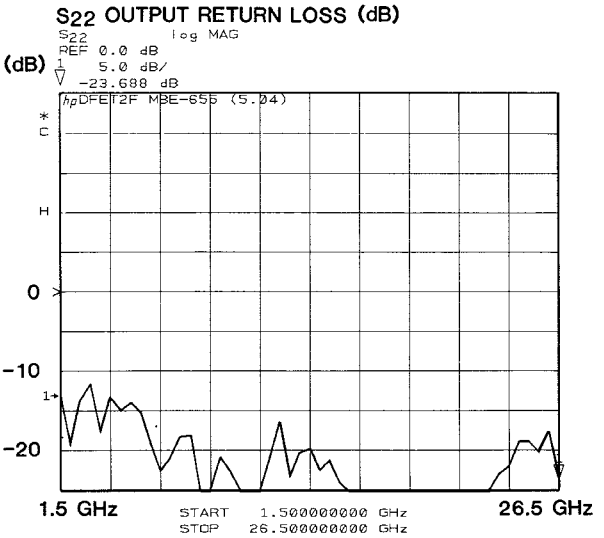
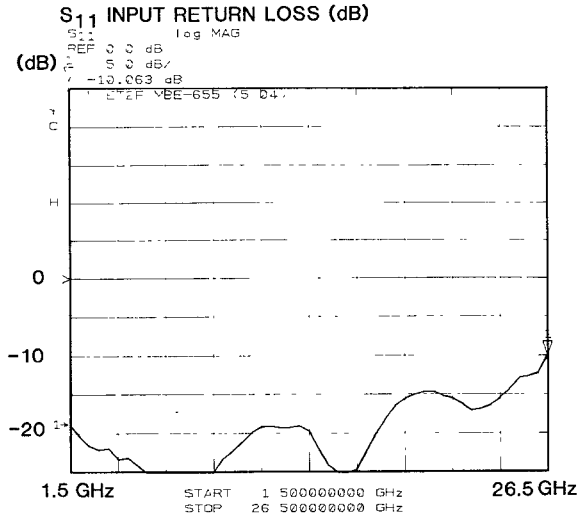
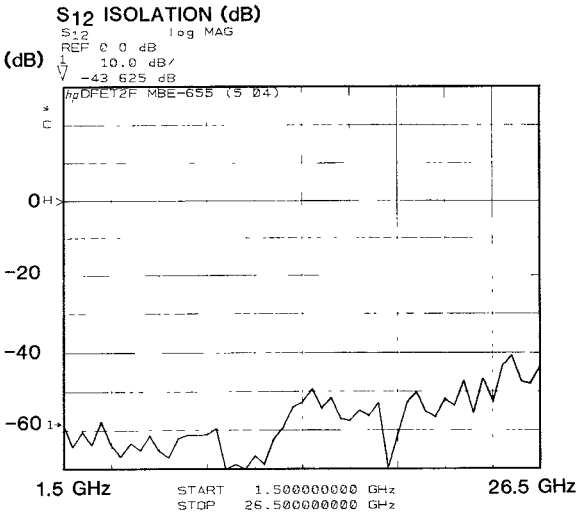








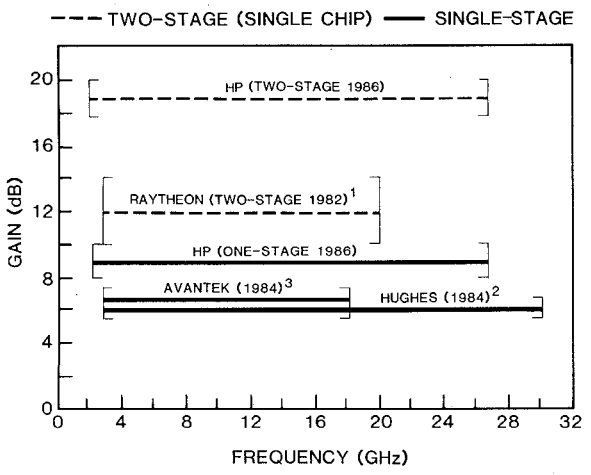
Bias Conditions

$V_{DD_A} = V_{DD_B} = 5.5$ Volts, $I_{DD_A} + I_{DD_B} = 328$ ma

$V_{G1_A} = V_{G1_B} = 0$ Volts, $V_{G2_A} = V_{G2_B} = 2.0$ Volts

Fig. 3 The four measured S-parameters of a DFET2F amplifier, measured on the wafer, with a Cascade-Microtech Model 42 probe station, connected to a Hewlett-Packard 8510A Network Analyzer.

The chart and table of Fig. 4 compares these results to previous results in the 2 to 30 GHz range. A 4 dB gain single chip distributed amplifier with flat gain to 40 GHz has been reported [4], using .25 μm gates with the same circuit as in reference [2].



REFERENCE	FREQ. RANGE	NO. STAGES	GAIN	INPUT, OUTPUT RETURN LOSSES	CHIP SIZE
Ref. 1	2-20GHZ	2	12±2dB	>6dB	2.2mm x 5.5mm
Ref. 2	2-30GHz	1	6±.3dB*	>12dB*	1.1mm x 3.2mm
Ref. 3	2-18GHz	1	6.3±.5dB	>10dB	.75mm x .85mm
This Work	1.5-26.5GHz	2	18.75±1.25dB	>12dB	1.62mm x 3.02mm

*Measured results presented covered 2-26.5GHz

Fig. 4 Gain of MMIC distributed amplifiers.

The DFET2F amplifier has a significantly higher gain for this size chip than any previously reported result. It consists of two identical DFET1F single stage sections cascaded in series.

Circuit Design

The design process of a DFET1F initially followed a procedure similar to those presented in previous works [5,6]. A cutoff of 32 GHz was chosen to assure performance to 26.5 GHz with FET parameter variations and temperature extremes. The design uses seven identical dual-gate FETs per stage, where the gate dimensions are 124 μm by 0.4 μm. Once the basic amplifier was designed, it was simulated on Super-Compact [9], with the length of the drain peaking line varied to compensate for losses along the gate line. Both the gate and the drain lines are terminated with 50 ohm thin-film resistors in series with on-chip bypassing capacitors. On-chip biasing networks bias the first gates to ground through a 1 kΩ resistor, and the second gates to $0.36 \cdot V_{DD}$ when external gate biases are not provided. Two DFET1F stages are coupled by a 12 pF capacitor shaped as a 50 ohm transmission line, to form a DFET2F amplifier. The layout of the DFET2F amplifier chip is shown in Fig. 5.

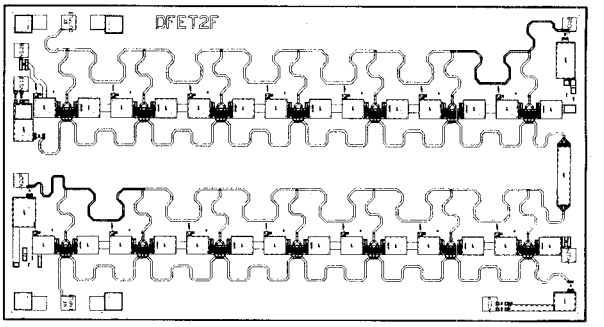


Fig. 5 DFET2F chip layout 3.02 mm x 1.62 mm.

Using dual-gate FETs gives 2 dB higher gain, and 6 dB more reverse isolation per stage [3]. However, previous experimental results with cascode distributed amplifiers had a tendency to oscillate near the cutoff frequency of the gate and drain artificial delay lines. The cascode pair is unstable when loaded with large inductive reactances at both the gate and the drain. Fig. 6 [7,8] shows the increase in impedance at the capacitor nodes of an artificial delay line filter, leading to instabiity.

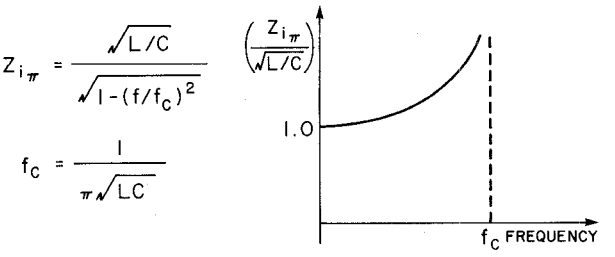


Fig. 6 Pi-section image impedance of an artifical delay line low-pass filter.

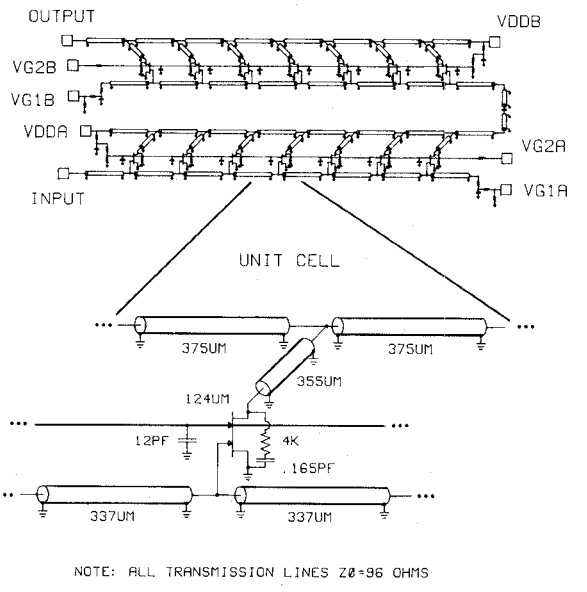


Fig. 7 DFET2F circuit schematic.

This problem has been solved by adding a simple R-C network in shunt with the drain of the common-gate FET, as shown in Fig. 7. The 4 kΩ resistor eliminates the drain line resonance near the cutoff frequency, and improves the gain flatness over the high end of the band, as shown by the computer simulation of Fig. 8. Without the 4 kΩ resistor (trace (a) in Fig. 8), the minimum stability K-factor was -29, and $|S_{22}|$ was 1.9 at 30 GHz. With the 4 kΩ resistor (trace (b)), the minimum stability K-factor was 20, and $|S_{22}|$ was .56 at 30 GHz.

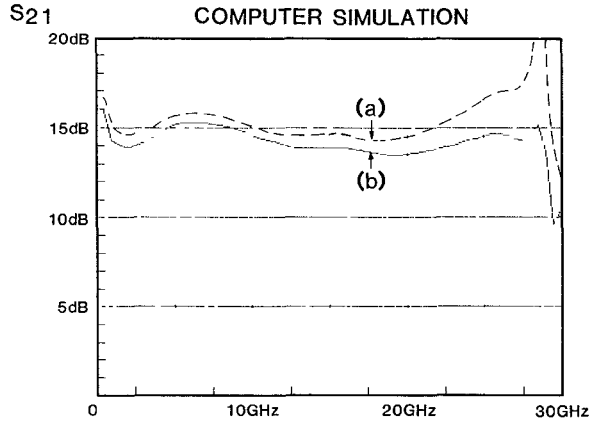


Fig. 8 Effect of damping resistor on gain flatness, (a) without 4 kΩ resistor (b) with 4 kΩ resistor.

Although the FET model used for the original design simulations had an f_t of 19 GHz, process improvements resulted in a FET with an f_t of 23 GHz, thereby accounting for the higher measured gain [10].

Circuit Fabrication

The MMIC process used for fabrication of the distributed amplifier described here is similar to a previously reported process [11], except for the following added features. The gate length is nominally 0.4 μm and patterned using deep-UV exposure [12]. The active layer was doped at $2 \cdot 10^{17}/cm^3$ grown using MBE. The f_t measured on a typical FET is 23 GHz. In addition, tantalum nitride thin-film resistors are available (25 ohms/square), as well as backside VIAs. The wafers are undoped LEC and 100 μm thick at the end of the process.

Conclusions

A two-stage, seven-section, dual-gate monolithic GaAs distributed amplifier with high gain and excellent flatness has been realized on a single MMIC chip. The instability problem associated with the cascode configuration has been solved, thereby allowing the superior gain and isolation properties of the dual gate FET to be utilized in distributed amplifiers.

Acknowledgments

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